Mark A. Taylor

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HARDWARE ENGINEERING DIRECTOR

Hardware Engineering Director focused on managing programs, disciplines, and processes across entire Product Lifecycle that brings systems to market and sustains them. Breadth spans component level through large complex systems. Expertise includes program and portfolio management, digital, electrical, mechanical, and low level software using multiple development and manufacturing business models at board, subsystem, and system levels. Experience in product development as well as manufacturing organizations supports optimizing the balance between Product Management, System Development, Manufacturing, Sustaining, Vendors, Customers, and Finance. Recognized for cross-discipline experience and enhancing partnerships across departments and companies for rapid development with high quality.

Key Skills include:

Engineering Management| Product Development | Systems Engineering | Portfolio Management
Program Management | Embedded Systems | HW Sustaining | Continuous Process Improvement
Vendor Partnerships | Customer Management | Cost Management Strategy | Tools development

PROFESSIONAL EXPERIENCE

NetApp, Sunnyvale, CA **April 2013 - October 2020**

Director, Hardware Engineering

Managed entire SSD and HDD primary storage drive portfolio and field inventory quality spanning 3 system product lines, from technology partnership and qualification through field reliability. Improved tools development, data tracking, and metrics analysis. Applied system development experience to improve outcomes.

- Drove material continuity, cost, and execution strategies in partnership with Product Management, System Development, Purchasing, and Manufacturing for optimized sourcing results across 6 active tier1 SSD/HDD suppliers that yielded head-of-line access to new technologies and multi-$10M savings from rapid access to new NAND generations.
- Provided portfolio management processes, tools, and organizational strategy that funneled options to plans which fulfilled supply continuity needs for continually increasing product complexity and count while staying within CAPEX budget at approximately flat head count including transitions to a lower cost area. More product at declining cost per quantity with same high enterprise quality.
- Monitored and enhanced metrics for early problem identification in production and field. Introduced drive internal parameter monitoring during qualification which lowered product volumes needed to catch problems and provided visibility to useful changes in qualification.

Managed central engineering department consisting of Mechanical Engineering, Power Engineering, Regulatory Engineering, Hardware Design and Hardware Sustaining groups which supported controller development and did shelf development.

- Managed development and introduction of new SAS storage shelf family using JDM model. Included ASSP expander chip change between builds without impacting schedule and staying within budget through strategy and partnership with JDM/SW/Mfg. Drove disk slot power/cooling specification and validation strategy, making future drive upgrades predictable.
- Led root cause analysis and corrective action of very low incidence midplane failure on previous product. Provided engineering customer communication based on the RCCA that saved large Japanese account.
- Analyzed system reliability and put processes in place to accelerate product maturity during development, resulting in lowered first year field failure rates. Drove fleet reliability analysis which provided early identification of emerging problems and delivered solutions in concert with field.

Themis Computer, Fremont, CA (Acquired by Mercury Systems) **January 2009 – March 2013**
Director, Engineering and Program Management
Managed programs, projects, and personnel to deliver Storage Servers, Rack Mount and Blade Servers, and Embedded Computers with extended temperature, vibration, and shock specifications.

- System definition to first customer ship of multi-module server in 3 months. Formalized process for customer builds out of engineering (previously ad hoc).
- Used projects to move organization from ad hoc to documented repeatable activities while retaining agility. Drove multiple development and manufacturing models - ground-up, full design through supplied-motherboard in custom enclosure.
- Managed development for rugged Themis designed storage server and Dell-EMC-partnered server.
- Architect and manager of ruggedized Blade Server development employing 10Gb Ethernet. Spec to working systems for sales conference in 8 months. OEM motherboards, PCIe cards, internal design for interconnect, 10Ge switch, service processor with custom firmware, and chassis/mechanicals.
- Directed program for extended temperature conduction cooled single board computer based VPX systems. Included development of single board computer module, chassis, IO modules. -40C to 70C ambient operating temperature with no internal fans.

Sun Microsystems, Menlo Park, CA **September 1996 – September 2008**
Senior Director Throughput Networking, September 2005 – September 2008
Managed development and sustaining of Sun branded Ethernet and cryptographic products for corporation. Development delivered ASIC, board, driver (Solaris, Linux, Windows), and FW for 10Gb and 1Gb Sun-designed Ethernet as well as Sun-branded third-party products.

Director, Value Engineering, October 2001 – September 2005
Reporting to SVP, World Wide Operations, identified material and manufacturing cost drivers, set benchmarks, and delivered capabilities that supported achieving costs including engineering services and negotiation support.

- Grew group from 8 to 25 in three-pronged approach to cost reduction – cost intelligence, supporting tool and process delivery, and re-engineering. Engineering disciplines in group: EE, ME, power, SI, board layout, ASIC, cost analysis, SW.
- Managed a portfolio of projects that leveraged an $8M budget to generate direct and indirect NPV savings of $45M and $100M+ respectively per year. Included DIMM redesign, mainframe class motherboard redesign including ASICs.
- Re-designed and influenced design of processor motherboards, power supplies, plastic and metal mechanicals, memory. Included mainframe class motherboard redesign with new ASICs.

Senior Manager, Thin Client Engineering, September 1996 - October 2001
Product Boss for network-attached Sun Ray and Javastation thin client projects. Negotiated and managed project with chosen Asian vendors. Managed OBP and diagnostic development.

EDUCATION

Bachelor of Science (BS) Electrical Engineering and Computer Science, University of California, Berkeley, CA

PROFESSIONAL DEVELOPMENT

Engineering Leadership Professional Program, University of California, Berkeley, CA

PATENTS

5,430,365 Power Regulation for Redundant Battery Supplies
5,455,935 Clock Synchronization System
5,678,005 Cable Detect Error Detection System
5,834,958 Power On System
5,948,111 Real Time Comparison of Integrated Circuit Operation